Amendments to the Specification:

Please replace line 10, page 4, paragraph **[0023]** with the following amended paragraph:

---**[0001]** During placement step ~~104~~ 103, a packing tool of the present invention groups the LUTs, registers, and other circuit blocks generated during technology mapping into logic blocks. Each logic block typically includes at least one LUT and at least one register. Logic blocks can be grouped into clusters of logic blocks such as a LAB on a programmable IC. A placement tool then places these logic blocks into actual logic blocks based on the geography of a programmable IC.---

Please replace on page 7, line 22, paragraph **[0042]** with the following amended paragraph:

---**[0002]** Figure 4 shows an example of a portion of a logic block. The logic block portion shown in Figure 4 illustrates examples of design rules that must be satisfied before an abstract block is placed into the logic block. The logic block of Figure 4 includes eight 3-input LUTs and 10 multiplexers that route output signals of the LUTs. The logic block also has two adder circuits 401 and 402 that are coupled together. ~~Adder circuit 401~~ Adder circuit 402 receives a carry input signal CIN from an adjacent logic block, and adder circuit 401 generates a carry output signal COUT that is transmitted to another adjacent logic block.---